AMENDMENTS TO THE CLAIMS

Please make the following amendments to the claims:

1. (Original) An interleaved generalized convolutional encoder, comprising:

(a) a node, the node being capable of receiving a data input, the data input being a portion of a data symbol;

(b) a memory element, the memory element being capable of storing a plurality of prior data inputs, the prior data inputs being a portion of each of a plurality of prior data symbols, the plurality of prior data inputs being subjected to a variable time delay; and

(c) a plurality of logic calculators,

(i) a portion of the plurality of logic calculators being capable of receiving a coefficient input,

(ii) the plurality of logic calculators including one or more final logic calculators, the one or more final logic calculators being capable of generating an output,

(A) the output being based on the data input, the plurality of prior data inputs, the plurality of logic calculators, the coefficient input, and the variable time delay.

2. (Original) The encoder of claim 1, wherein the data input is a portion of a PAM symbol.

3. (Original) The encoder of claim 1, wherein the data input is processed by a serial to parallel converter prior to entering the encoder.

4. (Original) The encoder of claim 1, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

5. (Original) The encoder of claim 1, wherein the variable time delay is a plurality of unit time delays.

6. (Original) The encoder of claim 1, wherein a receiver sets the variable time delay.

7. (Original) The encoder of claim 1, wherein a receiver dynamically sets the variable time delay.

8. (Original) The encoder of claim 7, wherein the variable time delay is based on the quality of a transmission path between a transmitter and the receiver.

9. (Original) The encoder of claim 7, wherein the variable time delay is based on noise affecting the transmission of data between a DTE and the receiver.

10. (Original) The encoder of claim 1, wherein the variable time delay is three bauds.

11. (Original) The encoder of claim 1, wherein the plurality of logic calculators includes a plurality of binary exclusive-OR gates and a plurality of binary AND gates.

12. (Original) The encoder of claim 1, wherein the output is processed by a mapper after exiting the encoder.

13. (Original) The encoder of claim 1, wherein the plurality of logic gates are implemented with firmware.

14. (Original) The encoder of claim 1, wherein the encoder is implemented with software that is executed with a processor.

15. (Original) The encoder of claim 1, wherein the variable time delay is implemented by a reference code of A=212124 octal and B=1202401 octal.

16. (Original) An interleaved generalized convolutional encoder, comprising:

(a) a variable time delay element;

(b) a switch;

(c) a plurality of convolutional encoders being capable of receiving a data input, the data input being a portion of a data symbol, wherein the data input is received by the switch and directed to one of the plurality of convolutional encoders based on the variable time delay element;

(d) the plurality of convolutional encoders being capable of storing a plurality of prior data inputs, the prior data inputs for any one of the convolutional encoders being a portion of each of a plurality of prior data symbols directed to the one of the convolutional encoders, the plurality of prior data inputs being subjected to a unit time delay; and

(e) a plurality of logic calculators associated with each of the plurality of convolutional encoders,

(i) a portion of the plurality of logic calculators being capable of receiving a coefficient input,

(ii) the plurality of logic calculators including at least one final logic calculator, the at least one final logic calculator being capable of producing an output,

(A) the output being based on the data input, the plurality of prior data inputs, the plurality of logic calculators, the coefficient input, and the variable time delay element.

17. (Original) The encoder of claim 16, wherein the data input is a portion of a PAM symbol.

18. (Original) The encoder of claim 16, wherein the data input is processed by a serial to parallel converter prior to entering the switch.

19. (Original) The encoder of claim 16, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

20. (Original) The encoder of claim 16, wherein a receiver sets the delay associated with the variable time delay element.

21. (Original) The encoder of claim 16, wherein a receiver dynamically sets the delay associated with the variable time delay element.

22. (Original) The encoder of claim 21, wherein the delay associated with the variable time delay element is based on the quality of a transmission path between a transmitter and the receiver.

23. (Original) The encoder of claim 21, wherein the delay associated with the variable time delay element is based on noise affecting the transmission of data between a DTE and the receiver.

24. (Original) The encoder of claim 16, wherein the delay associated with the variable time delay is three bauds.

25. (Original) The encoder of claim 16, wherein the plurality of logic calculators includes a plurality of binary exclusive-OR gates and a plurality of binary AND gates.

26. (Original) The encoder of claim 16, wherein the output is processed by a mapper after exiting the encoder.

27. (Original) The encoder of claim 16, wherein the plurality of logic gates are implemented with firmware.

28. (Original) The encoder of claim 16, wherein the encoding system is implemented with software that is executed with a processor.

29-30. (Cancelled)

31. (Currently Amended) A system for encoding information, comprising:

(a) first means for receiving a data input, the data input being a portion of a data symbol;

(b) second means for variably delaying a plurality of prior data inputs, the plurality of prior data inputs being a portion of each of a plurality of prior data symbols;

(c) third means for storing the variably delayed plurality of inputs;

(d) fourth means for performing logic calculations;

(e) fifth means for receiving a ~~receiver~~ coefficient input; and

(f) sixth means for producing an output, wherein the output is based on the operation of the first means, the second means, the third means, the fourth means, and the fifth means.

32. (Original) The system of claim 31, wherein the data input is a portion of a PAM symbol.

33. (Original) The system of claim 31, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

34. (Original) The system of claim 31, wherein a receiver determines the value of the variable delay of the means for variably delaying a plurality of inputs.

35. (Original) The system of claim 31, wherein a receiver dynamically determines the value of the variable delay of the means for variably delaying a plurality of inputs.

36. (Original) The system of claim 35, wherein a value of the variable delay is based on the quality of a transmission path between a transmitter and the receiver.

37. (Original) The system of claim 35, wherein a value of the variable delay is based on noise affecting the transmission of data between a DTE and the receiver.

38. (Original) The system of claim 31, wherein a value of the variable delay is three bauds.

39-49. (Cancelled)

50. (Original) A computer readable medium for encoding information, comprising:

(a) logic for receiving a data input, the data input being a portion of a data symbol;

(b) logic for variably delaying a plurality of prior data inputs, the plurality of prior data inputs being a portion of each of a plurality of prior data symbols;

(c) logic for storing the variably delayed plurality of prior data inputs;

(d) logic for performing logic calculations;

(e) logic for receiving a coefficient input; and

(f) logic for producing an output, the output being based on the operation of the logic for receiving a data input, the logic for variably delaying a plurality of prior data inputs, the logic for storing the variably delayed plurality of prior data inputs, the logic for performing logic calculations, and the logic for receiving coefficient input.

51. (Original) The system of claim 50, wherein the data input is a portion of a PAM symbol.

52. (Original) The system of claim 50, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

53. (Original) The system of claim 50, wherein a receiver determines the value of the variable delay of the logic for variably delaying a plurality of prior data inputs.

54. (Original) The system of claim 50, wherein a receiver dynamically determines the value of the variable delay of the logic for variably delaying a plurality of prior data inputs.

55. (Original) The system of claim 54, wherein a value of the variable delay is based on the quality of a transmission path between a transmitter and the receiver.

56. (Original) The system of claim 54, wherein a value of the variable delay is based on noise affecting the transmission of data between a DTE and the receiver.

57. (Original) The system of claim 50, wherein a value of the variable delay is three bauds.

58-77. (Cancelled)

78. (New) An interleaved generalized convolutional encoder, comprising:

a node configured to receive a data input, the data input being a portion of a data symbol;

at least one memory element configured to receive a series of data inputs from the node and to store the series of data inputs for a delay period, wherein the delay period is set by a remote receiver; and

a plurality of logic calculators, at least a first portion of the plurality of logic calculators configured to receive a coefficient input, and least a second portion of the plurality of logic calculators configured to generate an output based on the data input from the node and the stored series of data inputs from the memory element.

79. (New) The encoder of claim 78, wherein the delay period is based on the quality of a transmission path between the remote receiver and a local transmitter containing the convolutional encoder.

80. (New) An interleaved generalized convolutional encoder, comprising:

at least one memory element configured to receive a series of data input bits and further configured to output the oldest bit in the series after a delay of M symbol times, where M is greater than 1; and

at least one logic calculator configured to receive the oldest bit from the memory element and further configured to combine the oldest bit with a data input bit.

81. (New) The encoder of claim 80, wherein M is set by a remote receiver;

82. (New) The encoder of claim 81, wherein M is based on the quality of a transmission path between the remote receiver and a local transmitter containing the convolutional encoder.

83. (New) The encoder of claim 80, wherein the at least one logic calculator is further configured to receive a coefficient input.

84. (New) The encoder of claim 80, wherein the at least one logic calculator is further configured to use a coefficient input provided by a remote receiver.

85. (New) A method of interleaved generalized convolutional encoding, the method comprising the steps of:

receiving a data input bit X(m) at a first symbol time m;

storing the data input bit X(m);

receiving, after a delay of M symbol times where M is greater than 1, a data input bit X(m+M) at a second symbol time m+M;

outputting the stored data input bit X(m) at the second symbol time m+M; and

logically combining the data input bit X(m+M) and the outputted data input bit X(m).

86. (New) The method of claim 85, further comprising the step of:

receiving M from a remote receiver.

87. (New) The method of claim 86, wherein M is based on the quality of a transmission path between the remote receiver and a local transmitter containing the convolutional encoder.

88. (New) A transmitter comprising:

a serial-to-parallel converter configured to receive a first symbol in a first symbol period and a second symbol in a second symbol time separated from the first symbol time by M symbol periods, wherein the first symbol comprises a first plurality of bits and the second symbol comprises a second plurality of bits;

an interleaved convolutional encoder configured to interleave the at least one data bit in the first plurality and the at least one data bit in the second plurality and to logically combine the interleaved bits.

89. (New) The transmitter of claim 88, further comprising:

a mapper configured to receive the combined interleaved bits.